



Automotive Displays

The New SerDes Flagship in the APIX Fleet Reaches 12 Gbps

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Autor / Redakteur: Stefan Hoffmann, Fabian Kluge* / Johann Wiesböck

APIX3 enables infotainment architectures with 8K resolution and 10-bit RGB colour depth. The transmitter devices also enable video transmission via the VESA DisplayPort interface.



APIX has established itself as a de facto standard in the market over the past 13 years, with over 150 million nodes now installed. APIX is used by 10 OEMs in 60 models, and with APIX3 now also increasingly by Chinese manufacturers.

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The industry standard VESA DisplayPort differs from other video interfaces primarily in its high data rate, support for all common video formats up to and including 8K resolution and the possibility of transmitting several independent videos simultaneously. The DisplayPort interface is practically a de facto standard for powerful SoCs, such as those used in vehicles today. However, it was developed for consumer applications and not for the requirements of the automotive industry, which means that its use in vehicles poses major challenges.

Four independent differential lanes (4x2 cores), one differential AUX channel (1x2 cores) and a hot-plug detection signal

are required for signal transmission. Together, this results in at least eleven cable cores,

in addition to which there are usually configuration signals and ground connections that literally "add to the weight". The situation is similar with other video interfaces from the consumer sector, such as HDMI.

Therefore, to reduce the weight and the associated CO₂ emissions, but also the costs of multi-core cables, so-called SerDes solutions (serialisers/deserialisers) are used in the automotive industry, which bundle all signals and transmit them via a single pair of wires (2 cores). A widely used SerDes solution is the Automotive Pixel Link (APIX) from Inova Semiconductors. A broad portfolio of products has been on the market here since 2008, connecting SoC and display while at the same time meeting the high requirements of the automotive industry, such as reliable transmission and EMC.

APIX3 is the third device generation and offers a transmission rate of up to 6 Gbps per lane (coaxial or STP cable) or 12 Gbps via a Q(quad)STP cable. The INAP566/596TAQ transmitters are the latest products in the APIX3 family (Fig. 1). They have a DisplayPort 1.4a interface and enable video transmission rates of 2.7 Gbps (HBR) or 5.4 Gbps (HBR2). They also support Display Stream Compression (DSC), a VESA industry standard for lossless compression of video, so even high-resolution content can be transmitted in 4K at 120 fps or in 8K at 30 fps. The INAP596TAQ also supports the HDCP2.3 encryption standard.

The communication protocol is integrated

In addition to the DisplayPort, I²S, MII/RMII and SPI are also available to the user as further interfaces for communication and configuration. The data communication between the APIX components takes place via the integrated AShell. This is a communication protocol that has proven itself since the first APIX generation thanks to the built-in "zero-error" mechanisms. The AShell ensures that all communication data is transmitted error-free and integrated with other user data with the lowest possible latency.

The serial transmission of the pixel data takes place on two completely independent channels – with channel-specific CDR, fast-forward equalisation and dynamic sample point control – each of which provides a bandwidth of up to 6 Gbps in the downlink towards the display. In addition, each channel offers a bandwidth of up to 187.5 Mbps in the reverse direction to enable bidirectional, virtually latency-free communication for status, configuration and Ethernet data.

Thanks to echo cancellation, the bidirectional transmission takes place in full-duplex mode. Compared to other solutions that switch the communication direction, this mode offers the great advantage that no buffering of the serial data is necessary. This means that simultaneous real-time transmission can take place in both directions.

Automatic self and system calibration

As a very important feature, APIX3 has for the first time a fully automatic self and system calibration that covers all internal clock systems, as well as dynamically optimising the sample points. In addition, the line driver stages and filters are adjusted after each reset so that the frequency response of various cable types and lengths is compensated and these can be used via "plug and play". In addition, extensive diagnostic and compensation options are available to compensate for manufacturing tolerances, cable ageing and temperature effects.

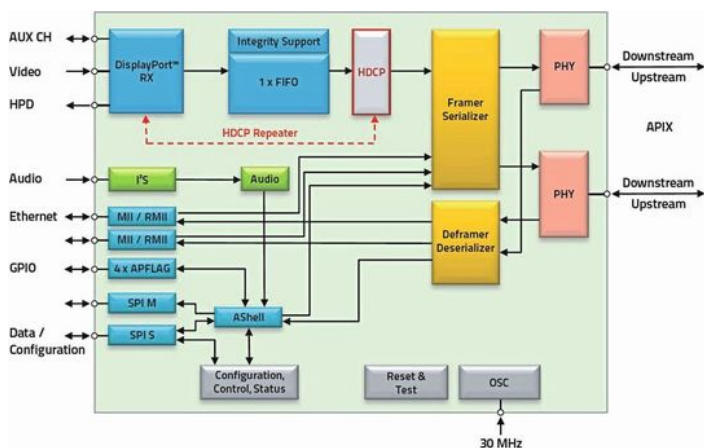


Fig. 1: The block diagram of the latest APIX3 transmitter INAP596TAQ with DisplayPort interface and 2 x 6 Gbps data rate: a highly integrated SoC with integrated microcontrollers for, among other things, fully automatic cable calibration and HDCP2.3 key management.

(Bild: Inova Semiconductors)

Since the first APIX generation in 2008, Inova Semiconductors has consistently used the "Non-Return-to-Zero (NRZ)" line code and "Current Mode Logic (CML)" with differential transmission. This method, which has been tried and tested in RF technology, is characterised by low emissions and high robustness against radiation.

In the APIX system, transmission takes place with a constant serial bit rate that is independent of the pixel rate of the videos to be transmitted. In terms of

radiation and interference immunity, the entire system can therefore be optimised for this frequency. Even when transmitting different video formats, the EMC behaviour remains almost unchanged.

12 Gbps bandwidth downstream

The APIX3 transmission system offers different operating modes and connection options between transmitter and receiver. In a "single lane mode", the transmitter is connected to the receiver device via a shielded twisted pair (STP) or coaxial cable.

Both lanes get interconnected in "Dual Lane Mode". For this application, quad-shielded twisted pair cables (QSTP) can be used in addition to the cable types mentioned. This mode provides up to 12 Gbps bandwidth for downstream transmission.

As already mentioned, a key feature of the DisplayPort interface is the ability to transmit multiple video streams independently of one another.



Fig. 2: Displays can be cascaded easily with the APIX3 repeater. Only one cable leads from the head unit to the display cluster; multiple image contents can be transported simultaneously via DisplayPort and APIX3. A significant saving in weight and costs.

(Bild: Inova Semiconductors)

chained" (Fig. 2). Only a single cable leads from the head unit to the display assembly – instead of the previous 4 to 6 cables with conventional star architectures. The first samples of the SC172x devices are expected to be available as early as the second quarter of 2022.

The new APIX3 devices INAP566/596TAQ from Inova are also – like all other APIX3 transmitters – fully downward compatible with the existing receiver devices of the APIX2 generation. This allows all video interfaces from the APIX portfolio to be combined with each other. In addition to DisplayPort, there are devices with HDMI and/or DSI (INAP56xTAQ) as well as LVDS or RGB interfaces (INAP375T/TAQ) on the transmitter side. LVDS or RGB (INAP37xR/RAQ), as well as DSI or CSI (INAP56xRAQ), are available on the display side.

For most interfaces, there are also device variants that support HDCP encryption (INAPx9x). In addition to the products from Inova Semiconductors, developers can also use the "Indigo" controllers from Socionext on the receiver side – now in the 4th generation since their launch in 2008. This ecosystem is unique in its diversity, combinability and backwards compatibility.

Against the background of the development of new receiver devices, such as the recently announced “Indigo 4” family from Socionext, this opens up completely new possibilities for future infotainment architectures. Socionext's SC172x smart display controllers will provide a repeater function for the first time, allowing multiple controllers to be cascaded and displays to be "daisy-

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The history of APIX

The number of displays is often more important to buyers than the number of cylinders

When APIX was introduced into vehicles in November 2008 with a great leap of faith from BMW – in the head-up display of the new 7 Series – the display landscape was still quite manageable. In addition to the innovative head-up display, instrument cluster and central display, there was also the rear-seat entertainment as an optional extra, and that was it. And the 1 Gbps data rate of APIX seemed amply dimensioned for the car and sufficient for a long time. Just 250 Mbps were needed to control the head-up display.



Robert Kraus, CEO Inova Semiconductors: "We are already thinking seriously about APIX4 today, with a native 24 Gbps transmission rate."

(Bild: 2021 by Timo Bierbaum)

rapidly and that the size and number of displays would often be more important to buyers than the number of cylinders. With the new architectures from 2025/26, where we are currently carrying out our design-ins with the APIX3 described in the adjacent article, we are talking about up to six displays on one head unit for the dashboard alone. And no longer "only" in full HD, but with 4k resolution; there is already talk of 8k displays – for use in cars, mind you.

APIX is now used by 10 OEMs in 60 models, and with APIX3 now also increasingly by Chinese manufacturers. Thanks to our ecosystem concept described in the article, APIX has established itself as a de facto standard in the market over the past 13 years, with over 150 million nodes now installed. And the development continues: after APIX, APIX2 and APIX3, we are already thinking seriously about APIX4 – with a native 24 Gbps transmission rate.

Four years later – APIX2 with 3 Gbps just had SOP – the four major German OEMs talked about the requirements of future high-speed networks and determined in a position paper from May 2012 that a data rate of up to 5 Gbps for display links would be sufficient for SOPs from 2018. But just one year later, when we were in the middle of the concept phase of APIX3, there were already the first rumours that two premium OEMs wanted to use full HD displays in cars in the future. Whereupon we discarded our original concept – more of an evolution of APIX2 – and started again from scratch with APIX3: with a break in the previous transmission concept, a new technology node, a new housing and a new ATE test concept.

However, no one could have imagined that infotainment in vehicles would develop so

Downward compatibility in particular offers the OEM a high degree of flexibility in platform development. This makes it possible to use a new SoC generation with higher performance and DisplayPort interface on the head unit, while an existing display platform can still be used on the receiver side. A changeover or upgrade can then be made at any time at a later date.

APIX ecosystem and compliance test

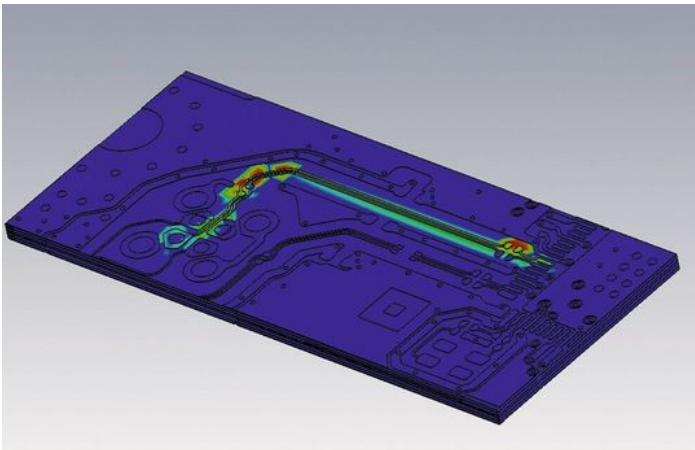


Fig. 3: For high signal integrity and noise immunity, the quality of the transmission line on the board is crucial. With a comprehensive 3D simulation, which Inova offers as a service, potential flaws in the board layout can be identified and easily corrected without having to manufacture the board first.

(Bild: Inova Semiconductors)

In the 13 years that APIX has now been on the market, over 150 million APIX nodes have been put on the road so far. Not only has Inova Semiconductors accompanied countless designs, but an extensive ecosystem has also emerged during this time. In addition to the large number of APIX components from several manufacturers, this also includes compliance tests for the board, recommendations for cable and connector systems, a precise specification of the requirements for the transmission channel and, in addition, extensive measurement technology from

leading manufacturers, some of which already has an "APIX button": here, the APIX specification is already firmly programmed into the scope. Inova Semiconductors also offers the simulation of customer designs with regard to signal integrity as a service in order to identify and remedy possible weaknesses in the design in the pre-series development (see Figure 3).

Modular developer boards are also available for all APIX components, with which the functions and interfaces of the components can be extensively evaluated (Fig. 4). The components are configured here using convenient configuration software with a user friendly GUI.

With the help of a special PHY monitor tool (Fig. 5), an eye diagram can be displayed on the receiver side in the real overall system in order to precisely evaluate jitter and noise on the signal. This makes it much easier to ensure highest signal integrity.



Fig. 4: With this modular developer platform, the APiX3-Link can be integrated into an existing system environment and evaluated. The video interface – such as DisplayPort on the Tx and DisplayPort, DSI or LVDS / oLDI on the Rx side – can be selected via piggyback boards. (Bild: Inova Semiconductors)

Experience from the APiX-PHY development was also applied in the development of the DisplayPort receiver and comparable diagnostic functions were incorporated. For user-friendly support, a software tool was therefore also developed for the DisplayPort, with the help of which eye diagrams of all four lanes can be created during operation. This allows the developer to analyse their board and minimise the likelihood of transmission errors occurring when receiving DisplayPort data.

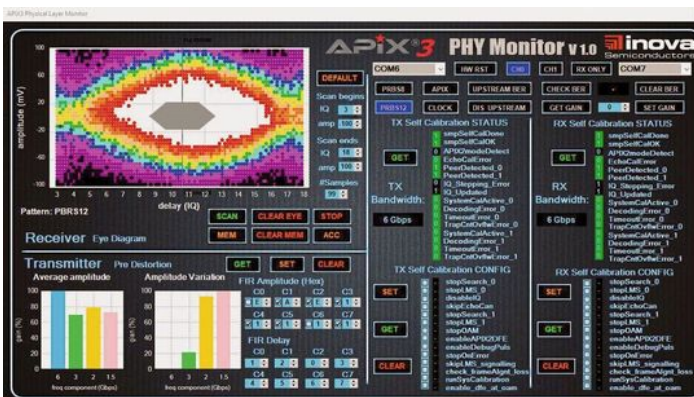


Fig. 5: For the final evaluation of the transmission system, the PHY monitor can be used to determine the quality of the incoming signal (jitter, level) exactly where it is relevant: not at a measuring point on the board, but directly at the RF input stage in the chip itself. This is made possible by a powerful eye-tracer algorithm. (Bild: Inova Semiconductors)

With the new flagship APiX3, Inova Semiconductors is continuing a success story that began with the market launch in 2008 and made APiX a de facto standard. The key to this, in addition to the consistent further development of the products, is the complete ecosystem that has emerged around APiX. Given the enormous complexity of today's infotainment systems, this is becoming increasingly important for developers.

* Stefan Hoffmann works as an application manager at Inova Semiconductors in Munich.

* Stefan Hoffmann works as an application

* Fabian Kluge also works in the application and prototyping department at Inova Semiconductors.

(ID:47397854)

KARRIERECHANCEN



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