APIX - 1st Generation

APIX® is Inova Semiconductors first Gbps Pixel Link, solving point to point connectivity solutions in the vehicle for display and camera applications. The APIX link transmits uncompressed pixel data with a sustained and resolution-independent link data rate of either 1 Gbps or 500 MBit/s over one single pair of STP copper cable. In addition to the pixel data, bidirectional sideband control data can be transmitted over the same pair of wires. The link supports distances of up to +15m (1 Gbps mode) and up to +40m (500 MBit/s mode) depending on the output settings and the cable properties.

Optimized for low EMI, the APIX link provides three independent channels for data transfer: the high speed downstream pixel channel, the downstream sideband channel, and the upstream sideband channel. The pixel channel and the downstream sideband channel are multiplexed and commonly transmitted over the downstream link. The upstream sideband channel can either be established over the same pair of wires as the downstream link (embedded upstream channel) or alternatively over a separate pair of wires. The configuration needs to be performed by the configuration vectors.

The bandwidth of the downstream link can be selected from two modes: “full bandwidth” mode with a link data rate of 1 Gbps, providing a net video data rate of 847 MBit/s, and “half bandwidth” mode with a link data rate of 500 MBit/s, providing a net video data rate of 423.6 MBit/s. The bandwidth also defines the maximum data rate possible for the sideband channels. The downstream sideband channel is transmitted in dedicated slots in the downstream link and therefore offers guaranteed low latency real-time characteristics. The maximum transmission rate is defined by the sampling frequency of the input pins. The upstream sideband channel is transmitted as differential signal on second twisted cable pair.

There are no external termination resistors required – for both Upstream and Downstream the dedicated 50 Ω termination resistors are integrated in the circuit.

APIX transmitter

The INAP125T24 is a transmitter for the Automotive PIXel (APIX) link for display and camera based point-to-point applications. The differential APIX link may be also used to supply power to the connected subsystem. Especially for cameras this feature is widely used to minimize cabling and connectors in the car.

The INAP125T14 video interface supports color widths of 10, 12, 18 and 24bit. The interface can be configured individually to match all popular display and image sensor interfaces. The pixel interface is
able to handle a wide spread pixel clock for lowest EMI. The APIX transmitter features dedicated high-speed outputs with adjustable drive current and pre-emphasis to facilitate the adaptation to different link distances and cable qualities while offering maximum data integrity and full EMI compliance to automotive standards such as CISPR25 and ISO11452-2. For optimized signal integrity and lowest EMI in dependence of the quality and length of the STP cable used, the output nominal current and the pre-emphasis current of the APIX transmitter can be set individually by means of external resistors.

The pixel data interface is the input for the 24 bit parallel pixel data representing the video data. In addition 3 pixel control signals like HSYNC, VSYNC and DE can be transmitted. The interface needs to be driven by an external pixel clock which acts as synchronous clock for the interface. The pixel clock is limited to 62 MHz. Data width and the configuration for the pixel control data are defined by configuration vectors. Pixel data and control signals are sampled with the pixel clock. The active edge can be configured to either rising or falling.

The sideband data upstream interface provides the sideband data at two (INAP125T24) output pins. The maximum data rate is limited by the upstream serial line clock, which is defined by a configuration vector.

The device parameters and settings of APIX transmitter and receiver are configured through a two-wire serial interface which is compatible to the MicroChip MicroWire™ interface. The configuration vectors can be provided through a microcontroller or out of a serial EEPROM. There is also a default initialization (camera mode) available in case there is no external configuration available.

**APIX receiver**

The INAP125R24 is a receiver for the APIX link. It supports video data widths of 10, 12, 18 and 24bit. The interface can be configured individually to match all popular display and image sensor interfaces. The pixel interface features spread spectrum staggered outputs for lowest EMI. The high-speed upstream outputs offer adjustable drive current to facilitate the adaptation to different link distances and cable qualities while offering maximum data integrity and full EMI compliance to automotive standards such as CISPR25 and ISO11452-2.

The INAP125R24 device offers some basic diagnostic features such as an automatic error detection for the downstream transmission, which can be configured and is actively indicated at an Error output pin. The INAP125R24 core clock frequency is generated by an internal PLL controlled by an external 10 MHz clock.

**AShell technology**

The APIX Automotive Shell (AShell) is an abstraction layer for the APIX Automotive PIXel Link Interface from Inova Semiconductors. It can be implemented as part of a system allowing a secure and error free data exchange on the bidirectional full duplex sideband channels of the standardized APIX link. This can be done in hardware or software and is part of the APIX Interface standard, which is supported by a number of chip suppliers such as Fujitsu, Toshiba and of course Inova Semiconductors APIX product family. A pixel (video) data stream of an application to be transmitted from TX to RX device is bypassed and thus not affected by the AShell layer.